



Yan, Q., Yuan, X., & Wu, X. (2016). A 100kHz 95.91% Efficiency SiC-device-based Split Output Converter with EMI Reduction. In *2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia 2016): Proceedings of a meeting held 22-26 May 2016, Hefei, China* [7512255] Institute of Electrical and Electronics Engineers (IEEE).
<https://doi.org/10.1109/IPEMC.2016.7512255>

Peer reviewed version

Link to published version (if available):
[10.1109/IPEMC.2016.7512255](https://doi.org/10.1109/IPEMC.2016.7512255)

[Link to publication record in Explore Bristol Research](#)
PDF-document

This is the author accepted manuscript (AAM). The final published version (version of record) is available online via IEEE at <http://ieeexplore.ieee.org/document/7512255/>. Please refer to any applicable terms of use of the publisher.

University of Bristol - Explore Bristol Research

General rights

This document is made available in accordance with publisher policies. Please cite only the published version using the reference above. Full terms of use are available:
<http://www.bristol.ac.uk/red/research-policy/pure/user-guides/ebr-terms/>

A 100kHz 95.91% Efficiency SiC-device-based Split Output Converter with EMI Reduction

Qingzeng Yan^{1,2}, Xibo Yuan¹, and Xiaojie Wu²

¹Department of Electrical and Electronic Engineering
University of Bristol
Bristol BS8 1UB, U.K.
Email: yqz2009@163.com

²School of Information and Electrical Engineering
China University of Mining and Technology
Xuzhou, Jiangsu 221116, China

Abstract—The adoption of silicon carbide (SiC) MOSFETs and SiC Schottky diodes in power converters promises a further improvement of the attainable power density and system efficiency, while it is restricted by several issues caused by the ultra-fast switching, such as phase-leg shoot-through (‘crosstalk’ effect), high turn-on losses, electromagnetic interference (EMI), etc. This paper presents a split output converter which can overcome the limitations of the standard two-level voltage source converters when employing the fast-switching SiC devices. The split output converter uses auxiliary inductors (called ‘split inductors’) to decouple the upper SiC MOSFET and the lower SiC MOSFET of the same phase leg, thus suppressing the crosstalk effect, improving the switching performance (e.g. lower turn-on losses), and reducing the EMI. However, there are also several issues brought by the split inductors, e.g. the current freewheeling problem, the current pulses and voltage spikes of the split inductors, and the disappeared synchronous rectification, which can together increase the losses of the converter. A 95.91% efficiency has been achieved by the split output converter at the switching frequency of 100kHz with EMI reduction.

Keywords—Silicon carbide (SiC); split output converters; crosstalk; efficiency; electromagnetic interference (EMI)

I. INTRODUCTION

The silicon carbide (SiC) MOSFETs have no tail current during switching, which characterizes the switching of Si IGBTs, resulting in a faster switching speed and dramatically reduced switching losses. The adoption of SiC MOSFETs enables the converters to operate at higher switching frequencies with reduced size and weight of the passive filters [1]. However, the converters with high switching speeds are more susceptible to the parasitic elements of the power circuits, e.g. the parasitic inductance of printed circuit board (PCB) traces and the parasitic capacitance of switching devices [2]. The high dv/dt and di/dt during the fast switching transient will bring serious electromagnetic interference (EMI) problem [3]. And the high dv/dt can intensify the interaction between the two complementary SiC MOSFETs of the same phase leg (crosstalk [4]).

Three key issues will emerge in the standard two-level voltage source converters with the fast-switching SiC devices [5], as illustrated in Fig. 1. Firstly, when the upper SiC MOSFET turns on, the Miller capacitance C_{gd} of the lower

SiC MOSFET will be charged inducing the spurious gate voltage, which may lead to the shoot-through failure of the converters (① in Fig. 1). Secondly, the output capacitance C_{oss} ($C_{oss}=C_{ds}+C_{gd}$, C_{ds} is the drain to source capacitance) of the lower SiC MOSFET will be charged during the upper MOSFET turn-on, increasing the turn-on losses of the upper SiC MOSFET (① and ② in Fig. 1). Thirdly, the intrinsic body diode of the SiC MOSFET tends to have higher reverse-recovery currents. If the body diode is used for freewheeling, its reverse recovery current can further increase the turn-on losses of the SiC MOSFET (③ in Fig. 1). Therefore, anti-parallel a better performance SiC Schottky diode is preferred in some applications [6]. However, even if the anti-parallel SiC Schottky diode features zero reverse recovery current, its output capacitance can still increase the total paralleled capacitance of the SiC MOSFET contributing to the turn-on losses [2].

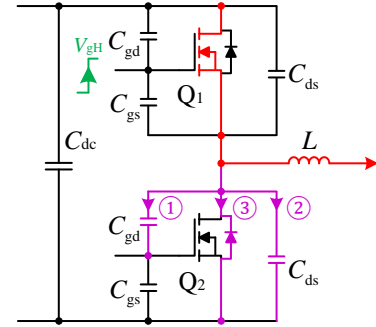


Fig. 1. Issues in standard two-level converters at the turn-on transient of the upper SiC MOSFET [①Charging the Miller capacitance C_{gd} , ②Charging the drain to source capacitance C_{ds} , ③Body diode reverse recovery].

The split output converters shown in Fig. 2 [7, 8], which are also known as the dual-buck converters [9], can transcend the above limitations of the standard two-level voltage source converters. In Fig. 2, $Q_1 \sim Q_6$ are SiC MOSFETs and $D_1 \sim D_6$ are SiC Schottky diodes; L_{load} is the load/filtering inductor. For the sake of clear description, the auxiliary inductors in split output converters, e.g. L_{s1} and L_{s4} , are called the ‘split inductors’. As seen in Fig. 2, the split inductors separate the upper SiC MOSFET from the lower SiC MOSFET, while the commutation loop remains low inductive to guarantee the fast switching speed. Consequently, with the split inductors the crosstalk effect will be suppressed with lower induced

spurious gate voltage avoiding the shoot-through failure. The charging current of the output capacitance and the reverse recovery current of the body diode will be both attenuated by the split inductors resulting in lower turn-on losses of the SiC MOSFET. In addition, if regarding the nodes O_a , O_b , and O_c in Fig. 2 as the outputs of the converter, the dv/dt of the output voltage will also be suppressed with mitigated EMI.

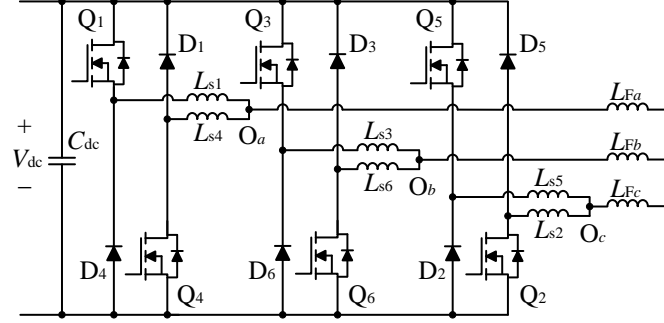


Fig. 2. The three-phase split output converter.

The split output converter could be one possible solution to overcome the new challenges in high-switching-frequency applications with wide bandgap devices [5, 7, 8]. However, there is still a lack of systematic and conclusive investigation into the split output converters regarding the crosstalk effect, the switching performance, EMI, and the specific issues of the split output converters, which should be concerned in high-switching-frequency applications. This paper therefore aims to carry out an experimental and analytical study, to reveal the advantages, disadvantages, and challenges of the high-switching-frequency split output converters with SiC devices.

II. DESIGNED SPLIT OUTPUT CONVERTER AND GATE DRIVE PULSE USED FOR DOUBLE PULSE TEST

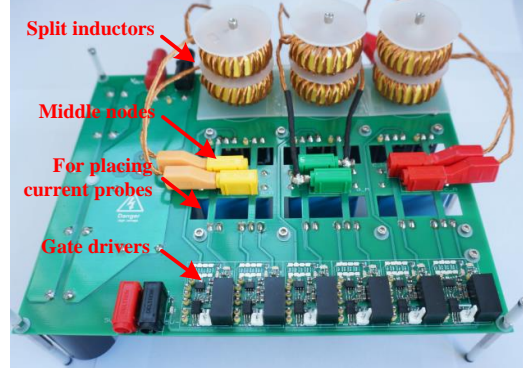
A. Designed Split Output Converter

A three-phase split output converter is designed with the scheme in Fig. 2, as shown in Fig. 3. The SiC MOSFET C2M0080120D (20A, 1200V, 80mΩ) and the SiC Schottky diode C4D20120A (20A, 1200V) both from Cree are used. The middle nodes shown in Fig. 3(a) are used to connect the split inductors of various values according to the requirements. The dc-link film capacitors in Fig. 3(b) are mounted closely to the switching devices for suppressing the current/voltage ringing generated by the high speed switching [10]. A differential voltage probe (N2790A, 100MHz) and a current probe (N2783A, 100MHz, 30A) both from Agilent Technologies are employed to measure the switching voltage and current.

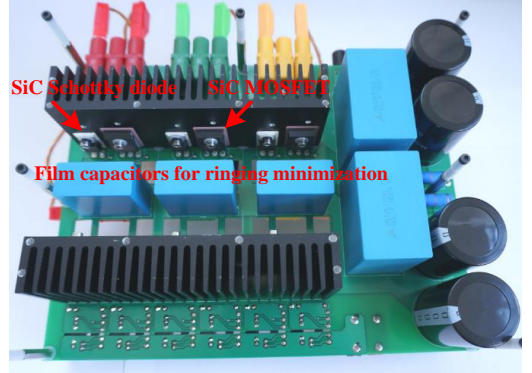
B. Gate Drive Pulse used for Double Pulse Test

In order to test some specific issues in split output converters, e.g. how the split inductors affect the synchronous rectification, the conventional gate drive pulse pattern used for double pulse test (DPT) [11] is modified in this paper as shown in Fig. 4. During the experiments, the period of each segment can be adjusted according to the requirements. The function of each segment is listed as follows:

- 1) $t_a \sim t_b$: Establishing the desired current level.
- 2) t_b and t_f : Testing the turn-off characteristic of the SiC MOSFET.
- 3) $t_b \sim t_c$ and $t_d \sim t_e$: Testing the current share between the SiC Schottky diode and the body diode of the SiC MOSFET.
- 4) $t_c \sim t_d$: Testing the current share between the channel of the SiC MOSFET and the diodes (the SiC Schottky diode and/or the body diode of the SiC MOSFET) in synchronous rectification mode.
- 5) t_e : Testing the turn-on characteristic of the SiC MOSFET.



(a)



(b)

Fig. 3. The designed three-phase split output converter: (a) top view and (b) bottom view.

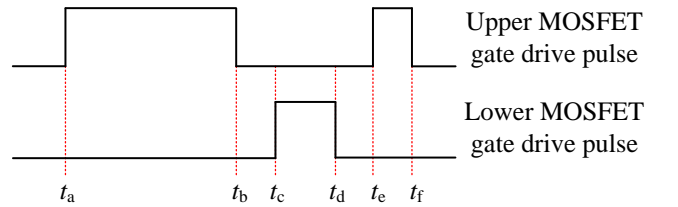


Fig. 4. Modified gate drive pulse used for DPT.

III. CROSSTALK ANALYSIS BASED ON A PROPOSED MODEL OF SPLIT OUTPUT CONVERTERS

In this section, a mathematical model of the split output converter is proposed to analyze the crosstalk effect. To simplify the analysis of the model, the parasitic inductance of the power circuits is neglected, and only the split inductance

and the parasitic capacitance of the devices are considered. The load is not analyzed here, though it can be added to the model if required. Taking Phase C of the split output converter for example, the circuit which can be used to analyze the Q_5 turn-on transient is shown in Fig. 5(a). The voltage source V_s in Fig. 5(a) represents the voltage at the middle node M of the left phase leg when Q_5 turns on. The parameters of the circuit are given in Table I. How the split inductance and the gate resistance influence the induced spurious gate voltage at the turn-on transient will be analyzed in the following.

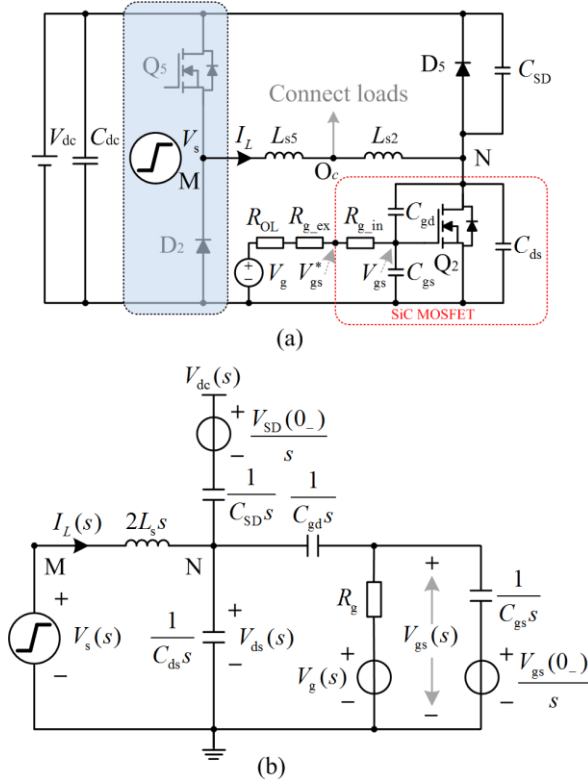


Fig. 5. Mathematical model of the split output converter: (a) circuit for the analysis of Q_5 turn-on transient and (b) equivalent circuit in s domain.

TABLE I. PARAMETERS OF THE MATHEMATICAL MODEL

Symbol	Parameter	Value
C_{SD}	Parasitic capacitance of SiC Schottky diode	80pF
C_{gd}	Miller capacitance of SiC MOSFET	6.5pF
C_{gs}	Gate to source capacitance of SiC MOSFET	943.5pF
C_{ds}	Drain to source capacitance of SiC MOSFET	73.5pF
R_{g_in}	Internal gate resistance of SiC MOSFET	4.6Ω
R_{OL}	Low-state output resistance of the gate driver	0.4Ω
R_{g_ex}	External gate resistance	Optional
V_{dc}	DC-link voltage	600V

The equivalent circuit of the split output converter in s (frequency) domain is shown in Fig. 5(b), where R_g is the total gate resistance ($R_g = R_{OL} + R_{g_ex} + R_{g_in}$); L_s refers to the split inductance, $L_s = L_{s1} = L_{s2}$; $V_{SD}(0_-)$ and $V_{gs}(0_-)$ are the initial

voltage on C_{SD} and C_{gs} , $V_{SD}(0_-) = V_{dc}$, $V_{gs}(0_-) = V_{gL}$ (V_{gL} is the low-state gate voltage). The initial voltages on C_{gd} and C_{ds} can be neglected compared to the voltages after they are fully charged (both approximately equal to the dc-link voltage after fully charged). To simplify the calculation, the piecewise voltage source $V_s(s)$ [12] is idealized as a step function. With the node-voltage method, selecting $V_{gs}(s)$ and $V_{ds}(s)$ as the node voltages, the circuit shown in Fig. 5(b) can be described as

$$\begin{cases} -C_{gd}sV_{ds}(s) + \left(C_{gd}s + \frac{1}{R_g} + C_{gs}s\right)V_{gs}(s) \\ = \frac{1}{R_g}V_g(s) + \frac{V_{gs}(0_-)}{s}C_{gs}s \\ \left(\frac{1}{2L_s s} + C_{ds}s + C_{gd}s + C_{SD}s\right)V_{ds}(s) - C_{gd}sV_{gs}(s) \\ = \frac{1}{2L_s s}V_s(s) + \left[V_{dc}(s) - \frac{V_{SD}(0_-)}{s}\right]C_{SD}s \end{cases} \quad (1)$$

where $V_g(s) = \frac{V_{gL}}{s}$ and $V_s(s) = V_{dc}(s) = \frac{V_{dc}}{s}$.

The gate voltage $V_{gs}(s)$ and the drain-source voltage of the SiC MOSFET $V_{ds}(s)$ can be derived from (1) as

$$\begin{aligned} V_{gs}(s) &= \frac{\frac{1}{2L_s s}V_s(s) + \left(\frac{1}{2L_s s} + C_{ds}s + C_{gd}s + C_{SD}s\right)\left(\frac{1}{R_g} + C_{gs}s\right)\frac{1}{C_{gd}s}V_g(s)}{\left(\frac{1}{2L_s s} + C_{ds}s + C_{gd}s + C_{SD}s\right)\left(C_{gd}s + \frac{1}{R_g} + C_{gs}s\right)\frac{1}{C_{gd}s} - C_{gd}s} \\ V_{ds}(s) &= \frac{1}{C_{gd}s} \left[\left(C_{gd}s + \frac{1}{R_g} + C_{gs}s\right)V_{gs}(s) - \left(\frac{1}{R_g} + C_{gs}s\right)V_g(s) \right]. \end{aligned} \quad (2)$$

The corresponding time domain values can be obtained by the inverse Laplace transform. It should be noted that V_{gs}^* in Fig. 5(a) is different from V_{gs} when the gate drive circuit is in the dynamic state. V_{gs}^* can be derived from V_{gs} using Ohm's law. The value of V_{gs}^* can be measured outside the device to compare with its theoretical value.

As seen in Fig. 5(a), after V_{ds} rises to V_{dc} , the split inductor current I_L will be freewheeled by the diode D_5 . At the time of V_{ds} rising to V_{dc} , V_{gs}^* will reach the maximum value $V_{gs_max}^*$ which can be taken as the spurious gate voltage. This time can be calculated by (3). Afterwards, the spurious gate voltage $V_{gs_max}^*$ at this time can be obtained from (2).

The theoretical results obtained from the model and the experimental results from the DPT with varying L_s and R_{g_ex} are shown in Fig. 6. $L_s = 0$ represents the case where no split inductors are used (as in a standard two-level converter). In order to minimize the influence of ringing on the experimental results, the external gate resistance of the switching SiC MOSFET Q_5 is selected as 33Ω which is relatively large, to slow down the switching speed for ringing suppression. The external gate resistance of the lower SiC MOSFET Q_2 is selected as required, e.g. varying from 6.2Ω to 100Ω. As seen in Fig. 6, the theoretical and experimental results generally

agree with each other. Due to some simplifications are made in the proposed model, e.g. the parasitic inductance of the power circuit is neglected and $V_s(s)$ is idealized as a step function, the measured spurious gate voltages have some discrepancies with the theoretical results.

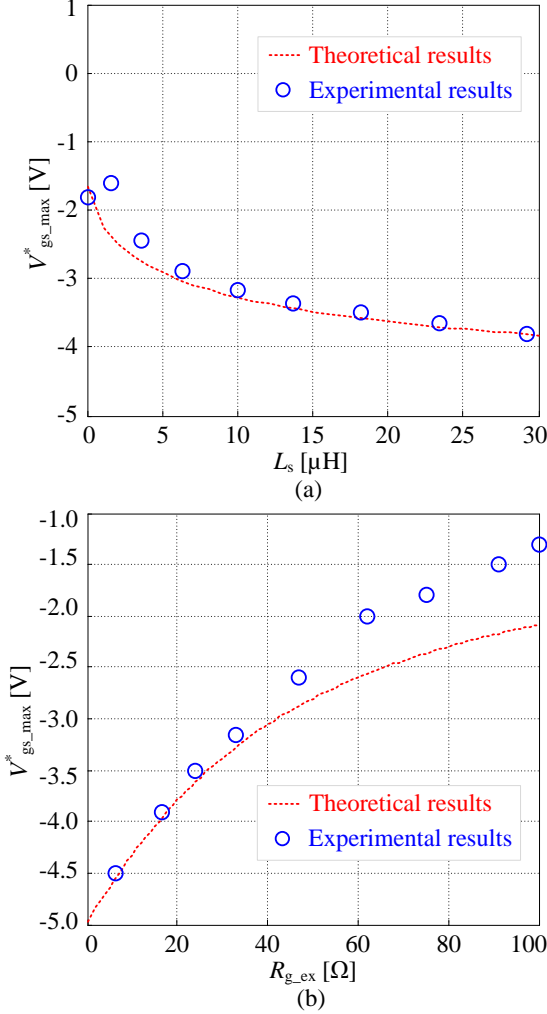


Fig. 6. Theoretical and experimental results of $V_{gs_max}^*$: (a) with varying L_s ($R_{g_ex}=33\Omega$) and (b) with varying R_{g_ex} ($L_s=10\mu H$).

As seen in Fig. 6(a), the induced spurious gate voltage $V_{gs_max}^*$ gradually decreases with the increasing split inductance. The phenomena can be simply explained as follows. Without the split inductors, V_s will directly charge the Miller capacitor C_{gd} with high spurious gate voltage. After the split inductors are added, the charging processes of C_{gd} is buffered with lower spurious gate voltage. Meanwhile, as seen in Fig. 6(b), $V_{gs_max}^*$ increases with the increasing external gate resistance R_{g_ex} , which can be explained based on the generation mechanism of the spurious gate voltage. During the charging process of the Miller capacitor C_{gd} , the charging current will also flow through C_{gs} and the resistance on the gate drive path, as seen in Fig. 5(a). The larger gate resistance will increase the parallel impedance of the gate resistance and C_{gs} , generating higher spurious gate voltage. Note that, even though the larger gate resistance can slow down the switching speed with reduced the spurious gate voltage, the increased

spurious gate voltage as analyzed above can outweigh the reduced spurious gate voltage, making the spurious gate voltage increase with the increasing gate resistance.

It should be also noted that, even if the low-state gate voltage is selected as -5V in this paper, the spurious gate voltage with a large external gate resistance and no split inductors can still be close to the gate threshold voltage of the SiC MOSFET ($V_{gs(th)}=1.7V$ for C2M0080120D). In contrast, the split inductors can effectively suppress the crosstalk with reduced spurious gate voltage preventing the potential shoot-through failure. The proposed model can be used as a reference for the selection of the external gate resistance and the split inductance.

IV. IMPROVED SWITCHING PERFORMANCE IN SPLIT OUTPUT CONVERTERS

In the switching performance test, a relatively small gate resistor of 6.2Ω is adopted to achieve a fast switching speed. The waveforms at turn-on and -off transients are respectively captured without and with split inductors, as show in Fig. 7.

Comparing Fig. 7(a) and Fig. 7(c), with the split inductors adopted, the turn-on current overshoot is reduced from 11A to 3A, and the low-frequency current ringing during the turn-on transient is suppressed. Comparing Fig. 7(b) with Fig. 7(d), the current and voltage distortions at the turn-off transient are smoothed by the split inductors. However, the split inductors have little influence on the high-frequency ringing of the current/voltage at both turn-on and -off transients. In addition, the turn-on energy is reduced from 920μJ to 725μJ by 195μJ, while the turn-off energy is increased from 100μJ to 180μJ by 80μJ.

In order to explain the phenomena, the circuit of the split output converter for DPT with parasitic elements considered is established as shown in Fig. 8, where L_{px} ($x=1, 2, 3 \dots$) is the parasitic inductance of the circuit; C_{p-L} is the parasitic capacitance of the load inductor; C_{oss} is the output capacitance of the SiC MOSFET, $C_{oss}=C_{ds}+C_{gd}$. The parasitic capacitances of the load inductor and the split inductor are measured by Wayne Kerr 65120B Precision Impedance Analyzer. The parasitic capacitance of the load inductor is 122.6pF, which is comparable with that of the devices, while the split inductor has a negligible parasitic capacitance of 2.1pF.

As seen in Fig. 8, the split inductors separate the switching MOSFET Q_5 from the parasitic capacitances of D_5 , Q_2 , and the load. The total parallel capacitance of Q_5 is dramatically reduced due to the addition of split inductors. The split inductors can effectively buffer the charge and discharge of the parasitic capacitors resulting in the reduced current overshoot in Fig. 7(c).

At the turn-off transient of Q_5 , the voltage change at M and N nodes will cause the charge and discharge of the capacitors. The current and voltage distortions shown in Fig. 7(b) are generated by the ringing in the charging/discharging processes [2]. Given the charging/discharging processes in the right phase leg and the load are buffered by the split inductors, the current and voltage distortions at the turn-off transient are suppressed, as shown in Fig. 7(d).

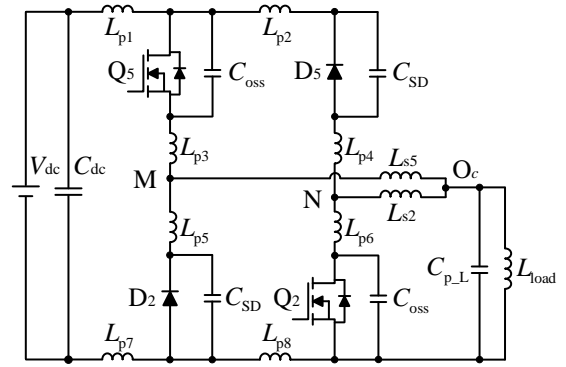
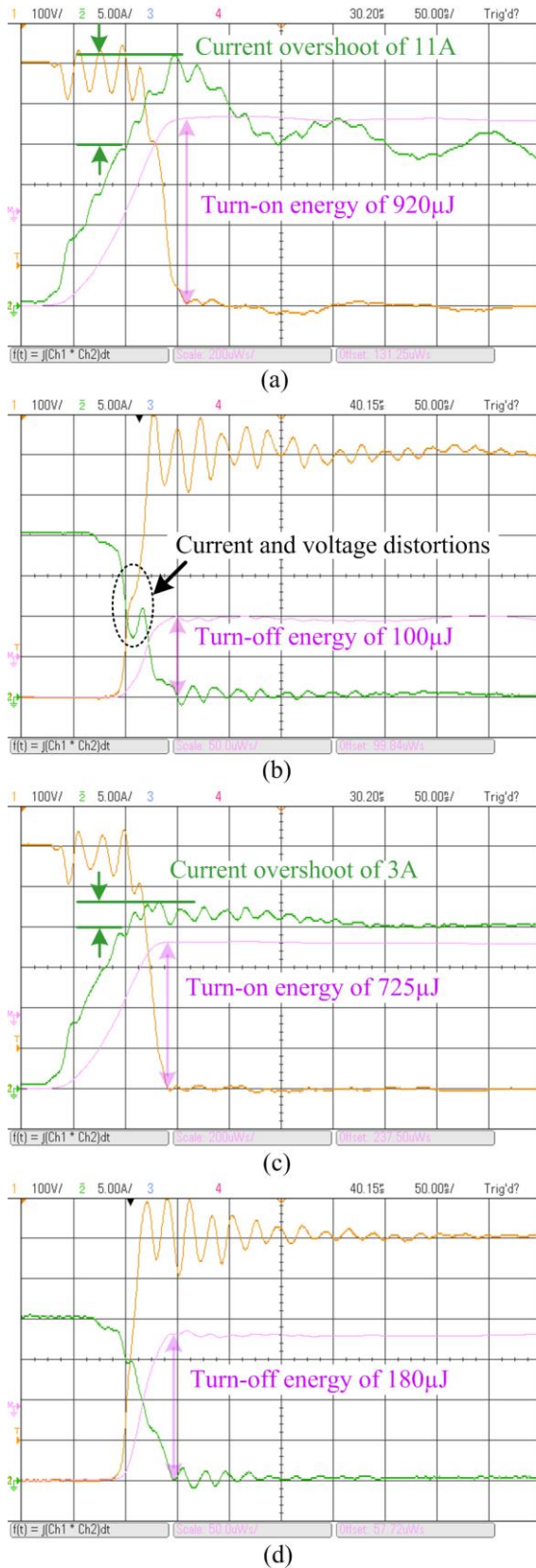


Fig. 8. Circuit of the split output converter for DPT with parasitic elements considered.

The low-frequency ringing in Fig. 7(a) is generated by the interaction between the parasitic inductance and the large parasitic capacitance in the right phase leg and the load. While the high-frequency ringing is caused by the parasitic inductance and the relatively small parasitic capacitance of the left phase leg. As seen in Fig. 8, the split inductor can block the charge/discharge of the parasitic capacitance in the right phase leg and the load, however, have no influence on the charge/discharge of the parasitic capacitance in the left phase leg. Therefore, the low-frequency ringing is effectively suppressed, but the high-frequency ringing cannot be affected.

Due to the fact that capacitors can slow down the voltage changing speed, after adding the split inductors, the reduced parallel capacitance of the SiC MOSFET enables the switching voltage to rise or fall faster, while the current changing speeds at the turn-on and -off transients both remain almost the same. This can be seen by comparing Fig. 7(a) with Fig. 7(c), and Fig. 7(b) with Fig. 7(d), respectively. Therefore, the current and voltage overlap area at the turn-on transient will be reduced with smaller turn-on energy, and the current and voltage overlap area at the turn-off transient will be increased resulting in larger turn-off energy. Moreover, there is a significant current overshoot during turn-on. With the faster voltage changing speed, the turn-on energy will be reduced significantly, which is higher than the increased turn-off energy, thus leading to an overall reduced switching energy.

V. EMI BENEFIT OF THE SPLIT OUTPUT CONVERTER

The voltage at the O_c node in Fig. 8, which can be treated as the output voltage of the split output converter, is measured with and without split inductors, as shown in Fig. 9.

Comparing Fig. 9(a) with Fig. 9(b), after applying the split inductors, the dv/dt at the rising and falling edges are reduced from 11.765kV/ μ s and 19.335kV/ μ s to 3.529kV/ μ s and 5.455kV/ μ s, respectively. And the voltage overshoot and undershoot, as well as the ringing of about 7MHz shown in Fig. 9(a) are effectively suppressed. These improvements in the output voltage of the split output converter can together lead to the EMI reduction.

To further compare the spectra of the output voltages, the DPT is repeated for 100 times, and the captured 100 output

voltage waveforms are synthesized into one signal to average the random noises. Then, the voltage spectra are computed by Discrete Fourier Transform (DFT). Fig. 10 shows the magnitude spectra of the output voltages without and with split inductors, which can clearly show the EMI benefit of the split output converter. As seen, the spectral amplitude between 3MHz and 25MHz is effectively reduced by the split inductors. Specifically, the reduced spectra magnitude around 7MHz can represent the suppressed ringing of about 7MHz in Fig. 9.

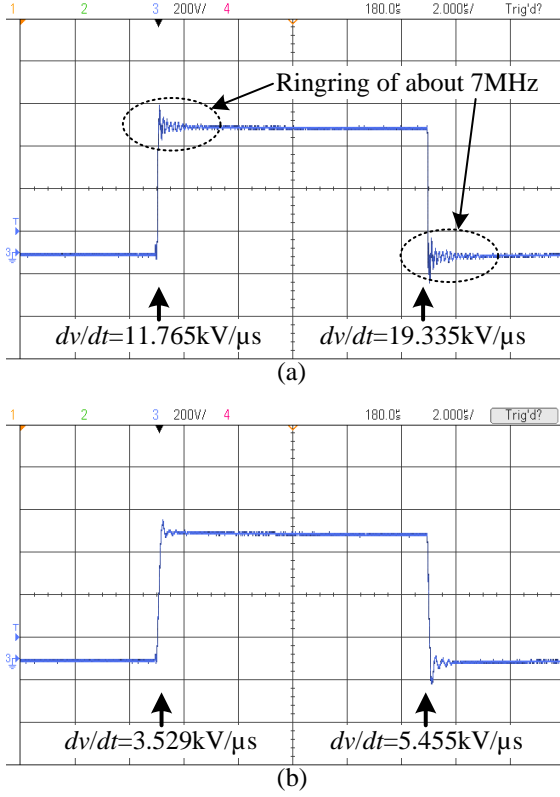


Fig. 9. Output voltage waveforms: (a) without split inductors and (b) with split inductors of 10μH.

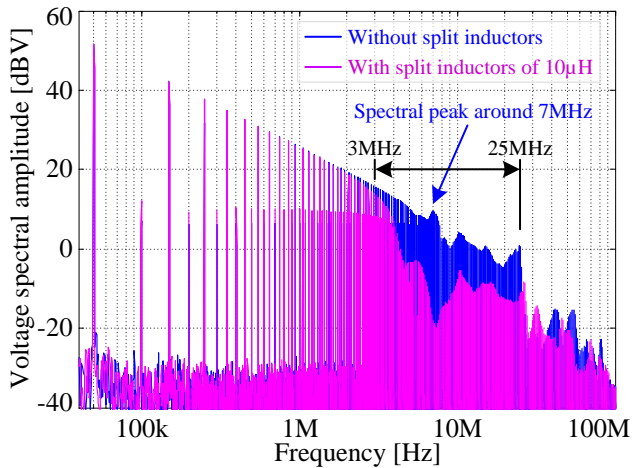


Fig. 10. Magnitude spectra of the output voltages without and with the split inductors of 10μH.

VI. SEVERAL ISSUES IN THE SPLIT OUTPUT CONVERTER

Apart from the above benefits of the split output converter, there are also several issues brought by the split inductors, e.g. the current freewheeling problem [7] and the current pulses and voltage spikes of the split inductors [8]. In addition, the split inductors can also make the synchronous rectification disappear.

The synchronous rectification is tested with and without the split inductors, respectively. The currents flowing through D_2 and Q_2 are measured and divided into three parts for clear descriptions, as shown in Fig. 11. As seen in Part 2 of Fig. 11(a) without split inductors, when Q_2 turns on, the current freewheeled by the SiC Schottky diode D_2 is partly switched to the channel of the SiC MOSFET Q_2 , making the circuit in the synchronous rectification mode. Fig. 11(b) shows the results with the split inductors of 10μH, the current of Q_2 in Part 2 has become very small, making the synchronous rectification mode almost disappeared.

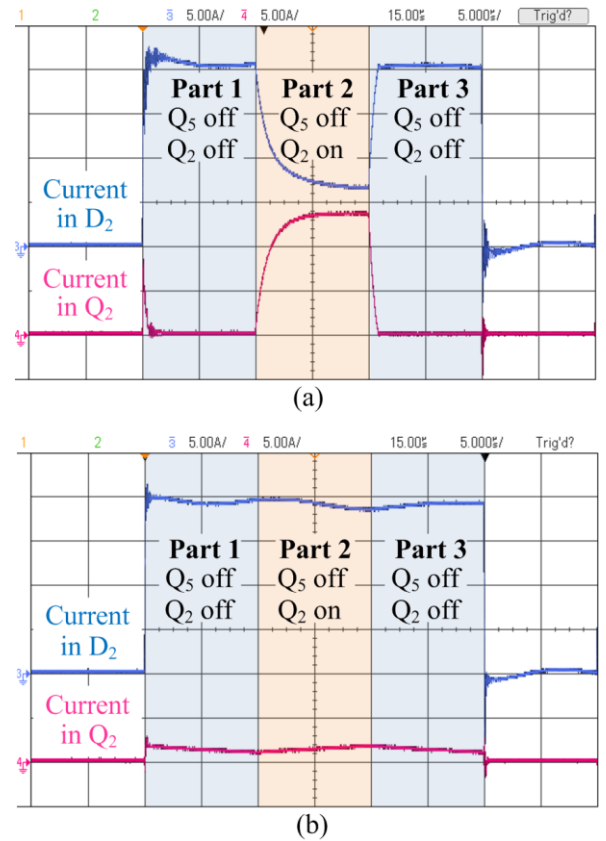


Fig. 11. Synchronous rectification: (a) without split inductors and (b) with split inductors of 10μH.

The reason why the synchronous rectification is affected by the split inductors can be given as follows. After Q_2 turns on, the circuit is in the synchronous rectification mode, where the current flowing through D_2 will fall while the current flowing through the channel of Q_2 will rise. At this time, the electromotive forces of the synchronous rectification path can be illustrated in Fig. 12. The falling current in the D_2 path will generate a forward-electromotive force V_{Ls5} on L_{s5} , which will

counteract the falling current in the D_2 path. Meanwhile, the rising current in the Q_2 path will generate a counter-electromotive force V_{Ls2} on L_{s2} , which will be against the rising current in the Q_2 path. How much current flowing through the channel of Q_2 depends on the voltage difference of $V_f - V_{Ls5} - V_{Ls2}$, where V_f is the voltage drop on the SiC Schottky diode D_2 . The split inductors associated with the rising and falling currents can generate the comparable electromotive force with V_f , making the synchronous rectification mode susceptible to the value of the auxiliary split inductors.

The disappeared synchronous rectification in the split output converter makes almost all the freewheeling current flow through the SiC Schottky diode. Given the equivalent on-state resistance of the SiC Schottky diode in parallel with the channel of the SiC MOSFET is smaller than that of a single SiC Schottky diode, the disappeared synchronous rectification can increase the conduction losses of the converter.

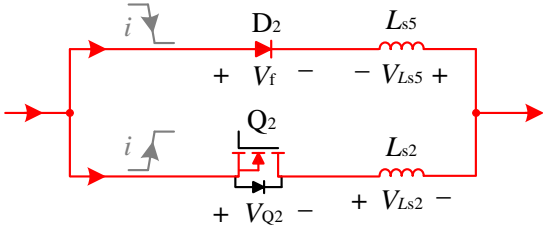


Fig. 12. Electromotive forces of the synchronous rectification path.

VII. EXPERIMENTAL RESULTS WITH CONTINUOUS OPERATION

The designed three-phase split output converter is tested in the continuous operation mode with a three-phase R - L load. The parameters of the system are given in Table II. The three-phase currents at the switching frequency of 100kHz without and with split inductors are shown in Fig. 13. As seen, the three-phase currents without split inductors in Fig. 13(a) have much larger high-frequency harmonics than the currents with split inductors in Fig. 13(b), which further verifies the EMI benefit brought by split inductors.

The efficiencies of the converter are measured without and with the split inductors at varying switching frequencies. The input dc power is calculated by the average dc current and voltage obtained by the oscilloscope. The output power is measured by the power analyzer NORMA 3000. The measured efficiencies and the corresponding operating power are shown in Fig. 14. It should be noted that, as the switching frequency increases, the voltage loss between the reference voltage and the actual output voltage caused by the dead time will also increase, leading to a reduced operating power. As seen in Fig. 14, the converter efficiencies with split inductors are always lower than those without split inductors at each switching frequency. This phenomenon is clear at the switching frequency of 100kHz, where the efficiency with split inductors is 0.73% lower than that without split inductors (95.91% vs. 96.64%).

Regarding the losses in the split output converter, the split inductor can lower the switching losses, which is expected in high-switching-frequency applications. However, the current

freewheeling problem [7] and the disappeared synchronous rectification (shown in Section VI) can together increase the conduction losses of the split output inverter. In addition, the current pulses and the voltage spikes of the split inductors can bring extra split inductor losses [8]. The overall increased conduction losses and split inductor losses can outweigh the decreased the switching losses, leading to the reduced efficiency of the output converter shown in Fig. 14. Further studies need to be carried out to optimize the efficiency of the split output converter to maximize its potential benefits in high-switching-frequency applications.

TABLE II. PARAMETERS OF THE TEST SYSTEM

Symbol	Parameter	Value
V_{dc}	DC-link voltage	600V
R_L	Load resistance	44 Ω
L_{load}	Load inductance	6.2mH
L_s	Split inductance	10 μ H
R_{g_ex}	External gate resistance	6.2 Ω
M	Modulation index	0.9
t_d	Dead time	1 μ s

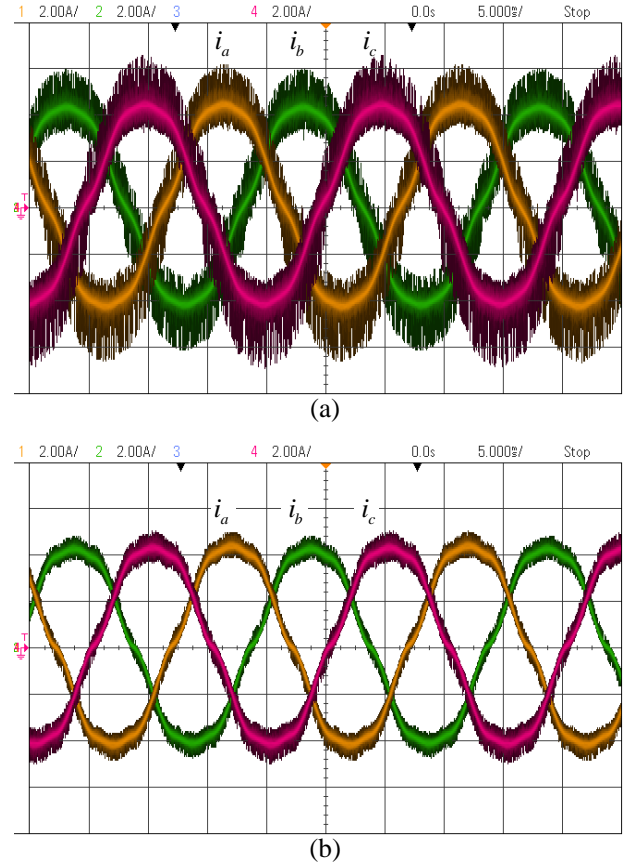


Fig. 13. Three-phase currents at switching frequency of 100kHz: (a) without split inductors and (b) with split inductors of 10 μ H.

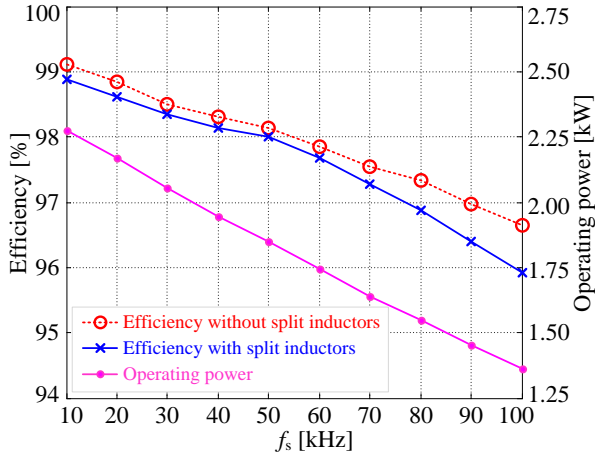


Fig. 14. Measured efficiencies without and with split inductors of 10 μ H, and the corresponding operating power.

VIII. CONCLUSION

A detailed investigation into the split output converter based on SiC MOSFETs and SiC Schottky diodes has been carried out both experimentally and analytically. The split output converter has both advantages and disadvantages. The switching performance is improved with lower turn-on current overshoot, suppressed low-frequency current ringing during the turn-on transient, and reduced current and voltage distortions at the turn-off transient. The reduced turn-on energy is higher than the increased turn-off energy leading to the reduced total switching losses. The EMI mitigation in the split output converter has been verified by the magnitude spectra of the output voltage and the experimental waveforms in the continuous operating mode. In addition, the split output converter has issues such as the current freewheeling problem, the current pulses and voltage spikes of split inductors, and the disappeared synchronous rectification, which need to be well addressed for the application of the split output converter. A 95.91% efficiency has been achieved by the split output converter at the switching frequency of 100kHz with EMI reduction.

Since the split output converter could be one possible solution to overcome the new challenges in high-switching-frequency applications with wide-bandgap devices, further studies need to be carried out to optimize the efficiency of the split output converter to maximize its potential benefits.

REFERENCES

- [1] J. Biela, M. Schweizer, S. Waffler, and J. W. Kolar, "SiC versus Si—Evaluation of potentials for performance improvement of inverter and DC–DC converter systems by SiC power semiconductors," *IEEE Trans. Ind. Electron.*, vol. 58, no. 7, pp. 2872–2882, Jul. 2011.
- [2] J. Wang, H. S.-H. Chung, and R. T.-H. Li, "Characterization and experimental assessment of the effects of parasitic elements on the MOSFET switching performance," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 573–590, Jan. 2013.
- [3] X. Yuan, S. Walder, and N. Oswald, "EMI generation characteristics of SiC and Si diodes: influence of reverse-recovery characteristics," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1131–1136, Mar. 2015.
- [4] Z. Zhang, F. Wang, L. M. Tolbert, and B. J. Blalock, "Active gate driver for crosstalk suppression of SiC devices in a phase-leg configuration," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1986–1997, Apr. 2014.
- [5] VINCOTECH. (Oct. 2013). SiC MOSFET-based power modules utilizing split output topology for superior dynamic behavior. [Online]. Available: http://www.vincotech.com/fileadmin/user_upload/articles/bp_2013_10-SiC_MOSFET-based_Power_Modules.pdf
- [6] B. Ozpineci, M. S. Chinthavali, L. M. Tolbert, A. S. Kashyap, and H. A. Mantooth, "A 55-kW three-phase inverter with Si IGBTs and SiC Schottky diodes," *IEEE Trans. Ind. Appl.*, vol. 45, no. 1, pp. 278–285, Jan./Feb. 2009.
- [7] H. Li, S. Munk-Nielsen, S. Bęczkowski, and X. Wang, "SiC MOSFETs based split output half bridge inverter: current commutation mechanism and efficiency analysis," in *Proc. Energy Convers. Congr. and Expo.*, Pittsburgh, PA, Sep. 2014, pp. 1581–1588.
- [8] S. Bęczkowski, H. Li, C. Uhrenfeldt, E.-P. Eni, and S. Munk-Nielsen, "10kV SiC MOSFET split output power module," in *Proc. 17th Eur. Conf. Power Electron. Appl.*, Geneva, Sep. 2015, pp. 1–7.
- [9] P. Sun, C. Liu, J.-S. Lai, C.-L. Chen, and N. Kees, "Three-phase dual-buck inverter with unified pulsewidth modulation," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1159–1167, Mar. 2012.
- [10] J. Fabre, P. Ladoux, and M. Piton, "Characterization and implementation of dual-SiC MOSFET modules for future use in traction converters," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4079–4090, Aug. 2015.
- [11] S. Tiwari, T. Undeland, S. Basu, and W. Robbins, "Silicon carbide power transistors, characterization for smart grid applications," in *Proc. IEEE 15th Int. Power Electron. Motion Control Conf.*, Novi Sad, Sep. 2012, pp. 2–1–2–8.
- [12] T. Wu. (2007). "Cdv/dt induced turn-on in synchronous buck regulations," International Rectifier, Tech. Rep. [Online]. Available: <http://www.irf.com/technical-info/whitepaper/synbuckturnon.pdf>